Baud-Rate Timing Recovery

Inventors

Eunjoo Hwang
Jongsang Choi
Deog-Kyoon Jeong

Matter Number: 4683

Prepared by:
C. Eric Schulman
Reg. No. 43,350
Fenwick & West LLP
Two Palo Alto Square
Palo Alto, CA 94306

Express Mail No.: EL482472478US

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CROSS-REFERENCES TO RELATED APPLICATIONS

This application relates to U.S. patent application serial no. 60/176,416, entitled "Baud-Rate Timing Recovery," filed on January 14, 2000, which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to data communication systems and methods. More particularly, this invention relates to a system and method for timing recovery.

2. Description of the Background Art

Communication systems increasingly depend on digital data transmission. Digital data transmission, in turn, depends on reliable reception of transmitted data. Effective timing recovery facilitates reliable reception of transmitted data in a digital data receiver. More specifically, effective timing recovery facilitates correct sampling instances of the received data stream. In other words, certain digital data receivers continuously adjust the frequency and phase of the receiver clock to optimize the sampling instants of the received data signal and to compensate for frequency drifts between the oscillators used in the transmitter and receiver clock

circuits.

A receiver can derive the timing information from the data signal itself. There are at least three timing recovery methods that recover timing information from the data signal. A first method detects the zero-crossing points of sampled data. See B. R. Saltzberg, "Timing recovery for synchronous binary data transmission," *Bell System Technical Journal*, vol.46, pp.593-622, Mar. 1967, which is incorporated herein by reference in its entirety. A receiver determines the sampling points as the mid-point between two adjacent crossings. This mid-point likely coincides with the maximum eye opening in an eye diagram. As is well known in the art, a display, e.g., an oscilloscope, connected to a demodulated, filtered symbol stream, can generate an eye diagram. The display retriggers at every symbol period or fixed multiple of the symbol period using a symbol timing signal derived from the received waveform to produce the eye diagram.

A second method exploits the signal derivatives at the sampling instants. See H. Kobayashi, "Simultaneous adaptive estimation and decision algorithm for carrier modulated data transmission systems," *IEEE Trans. Communications*, vol. COM-19, pp. 268-280, Jun. 1971; R. D. Gitlin and J. Salz, "Timing recovery in PAM systems," *Bell System Technical Journal*, vol. 50, pp. 1645-1669, May-June 1971, which are both incorporated herein by reference in their entirety. This method adjusts the sampling phase until the signal derivative at the sampling instant is zero, at which point, the method samples the data symbols at their peaks.

A third method involves applying a non-linear operation, such as squaring, to the received filtered data stream. The non-linear operation generates a signal with a strong, discrete frequency component, e.g., a spectral line, at the symbol timing frequency. A subsequent filtering operation with a sharp bandpass filter extracts the frequency of the symbol clock. See W. R. Bennett, "Statistics of regenerative digital transmission," *Bell System Technical Journal*,

vol.37, pp.1501-1542, Nov. 1958; Y. Takasaki, "Timing extraction in baseband pulse transmission," *IEEE Trans. Communications*, vol. COM-20, pp. 877-884, Oct. 1972; L. E. Franks and J. P. Bubrouski, "Statistical properties of timing jitter in a PAM timing recovery system," *IEEE Trans. Communications*, vol. COM-22, pp.913-920, Jul. 1974, which are all incorporated herein by reference in their entirety.

Many baud timing recovery systems use only one sample per baud interval, i.e., they use baud sampling. The information used by the timing recovery methods described above is not available with baud sampling. For example, with respect to the first method described above, a receiver performing baud sampling does not detect signal crossings with any useful precision. Unfortunately, the use of higher sampling rates or additional sampling of the signal derivative for timing recovery is not an appealing solution because of the corresponding increase in expense, complexity, and amount of hardware.

Kurt H. Muller and Markus Muller introduced a baud-rate timing recovery scheme which exploits a timing function based on sampled data and estimated data values. The output of the timing function determines the sampling instants. See "Timing recovery in digital synchronous data receivers," *IEEE Trans. Communications*, vol. COM-24, no.5, pp. 516-531, May 1976 which is incorporated herein by reference in its entirety. The success of the scheme depends on how accurately it can estimate the received data. Hence, when using a channel that severely distorts the transmitted signal, the Muller and Muller scheme can fail to operate properly without a training sequence.

When using a channel that severely distorts the transmitted signal, an automatic equalizer is useful to compensate for the distortion. However, if the system does not incorporate a training sequence, the automatic equalizer will not accurately estimate the incoming data values until the equalizer settles. As noted above, the timing function is a function of the

estimated data values and the timing function determines the timing of the sampling instants. Thus, the timing of the sampling instants drifts until the equalizer settles if the timing recovery system uses a timing function that is a function of the sampled data values and the estimated data values. Furthermore, when the timing of the sampling instants drifts the equalizer typically does not achieve stable operation. Consequently, joint operation of the equalizer and the timing recovery system is needed.

U.S. Patent No. 3,697,689 to E.D. Gibson, entitled "Fine timing recovery system," which is incorporated herein by reference in its entirety, describes one such method, i.e., a method that provides joint operation of the equalization and the timing recovery. The Gibson patent describes using tap coefficients of a linear zero-forcing equalizer with a transversal filter configuration, where if the channel impulse has a peak value, the tap coefficients also have a peak value. The method that Gibson describes adjusts the timing until the main tap coefficient is located at the peak of the impulse response. However, this method inherits the traditional problems present in a linear equalizer, such as noise enhancement.

Expanding on noise enhancement in a linear equalizer, one can represent the input to a linear equalizer as $x(n) = \sum_i h(i)a(n-i) + N(n)$. In the above equation, the first term includes inter-symbol interference (ISI) and the second term represents Gaussian noise. A linear equalizer removes ISI not Gaussian noise. A linear equalizer includes a number of taps, each tap time delayed relative to its neighbor, the taps measuring the input. The equalizer multiplies the output of the taps by coefficients and sums the resulting terms. Thus, the equalizer also multiplies the Gaussian noise term in the input by the same coefficients and sums the resulting terms to increase the noise power. Consequently, Noise power is proportional to the number of taps.

Therefore, there is a need for improved systems and methods for timing recovery. There is a need for timing recovery systems with reduced noise enhancement. There is also a need for timing recovery systems that coordinate equalization and timing recovery.

SUMMARY OF THE INVENTION

The present invention provides baud-rate timing recovery methods and systems for recovering timing information from a transmitted signal. Versions of the invention combine timing recovery with equalization. One embodiment achieves the equalization using a decision feedback equalizer (DFE). A DFE enjoys wide popularity in digital data receivers because of its superior performance, relative to a transversal filter, in reducing inter-symbol interference (ISI). See Edward A. Lee and David G. Messerschmitt, *Digital Communication*, Kluwer Academic Publishers, 1994; C. A. Belfiore and Jr. J. H. Park, "Decision feedback equalization," *Proc. IEEE*, vol.67, pp.1143-1156, Aug. 1979, which are both incorporated herein by reference in their entirety.

A DFE typically comprises a feed-forward filter (FFF) and a feedback filter (FBF) for reducing pre-cursors and post-cursors of the channel impulse response, respectively. Under the zero-forcing condition, the coefficients of a FFF and of a FBF are functions of the channel impulse response. Applying simple arithmetic operations to those coefficients obtains several timing functions. One can define a timing function as the expected timing update that, for example, the timing recovery system converts to a voltage to control a VCO in a PLL. The VCO, in turn, controls the sampling phase of a sampler in the timing recovery system.

One of the most widely known timing functions for binary data is as follows:

$$E\{z_k\} = \frac{1}{2}E\{x(k)a(k-1) - x(k-1)a(k)\} / E\{a(k)^2\} \qquad (1)$$

$$= \frac{1}{2}(h(1) - h(-1)) \qquad (2)$$

where *x(k)* is the k-th sample of received data, *a(k)* is the estimation of *x(k)*, and h(1) is the first post-cursor and h(-1) is the first pre-cursor. One can define the timing function $f(\tau_k) = E\{z_k\}$, where z_k is a stochastic function of the timing error in the kth sample, τ_k. If one substitutes

$$x(k) = \sum_i h(i)a(k-i) \quad \text{and} \quad E\{a(m)a(n)\} = \begin{cases} E\{a(m)^2\} & m = n \\ 0 & otherwise \end{cases}, \text{ (1) will result in (2).}$$

When the channel impulse response is symmetrical, the optimum sampling instance is reached at the peak point of the impulse response, where $E\{z_k\}$ is 0.

When the channel impulse response is not symmetrical, the optimum sampling point can be reached by scaling the terms in equation (1) as follows:

$$E\{z_k\} = \frac{1}{2} E\{\alpha x(k)a(k-1) - \beta x(k-1)a(k)\} / E\{a(k)^2\}. \qquad (3)$$

For more information on scaling the timing function, see Peter Gysel and Dietrich Gilg, "Timing recovery in high bit-rate transmission systems over copper pairs," *IEEE Trans. Communications*, vol.46, no.12, pp.1583-1586, Dec. 1998, which is incorporated herein by reference in its entirety.

However, in a severely distorted channel, the estimated values, *a(k)* and *a(k-1)*, are not available until the equalizer compensates for the channel distortion. As a consequence, a training sequence is needed for both the equalizer and the timing function.

Thus, rather than use the above-referenced configurations and timing functions, one version of the present invention provides a sampler, a DFE, and a timing error detector. The sampler has first and second inputs and an output. The first input receives a transmitted signal. The second input receives a clock signal. The sampler operates to sample a transmitted signal according to the clock signal.

The DFE has an input and first and second outputs. The input couples to the output of the sampler. The DFE has a first pre-cursor tap providing the first output and a first post-cursor

tap providing the second output.

The timing error detector has first and second inputs and an output. The first input couples to the first output of the DFE and the second input couples to the second output of the DFE. The timing error detector operates to provide at the output a signal representative of the timing error reflected in the sampled transmitted signal. The clock signal at the second input of the sampler is derived using the signal provided at the output of the timing error detector.

Another version of the invention provides a baud-rate timing recovery method for recovering timing information from a transmitted signal. The method includes sampling a transmitted signal using a sampler having first and second inputs and an output. The first input receives a transmitted signal. The second input receives a clock signal. The sampler operates to sample a transmitted signal according to the clock signal;

The method further includes equalizing the sampled, transmitted signal using a DFE. The DFE has an input and first and second outputs. The input couples to the output of the sampler. The DFE has a first pre-cursor tap providing the first output and a first post-cursor tap providing the second output.

The method also includes deriving a signal representative of a timing error reflected in the sampled, transmitted signal using a timing error detector. The timing error detector has first and second inputs and an output. The first input couples to the first output of the DFE and the second input couples to the second output of the DFE. The timing error detector operates to provide the signal representative of the timing error at the output. The clock signal at the second input of the sampler is derived using the signal provided at the output of the timing error detector.

The features and advantages described in this summary and the following detailed description are not all-inclusive, and particularly, many additional features and advantages will

be apparent to one of ordinary skill in the art in view of the drawings, specification, and claims hereof. Moreover, it should be noted that the language used in the specification has been principally selected for readability and instructional purposes, and may not have been selected to delineate or circumscribe the inventive subject matter, resort to the claims being necessary to determine such inventive subject matter.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a decision feedback equalizer.

Figure 2 is a plot of impulse response of the 100m UTP Category-5 cable with external effects.

Figure 3 is a plot of the output of the timing functions.

Figure 4 is a block diagram of a preferred embodiment of the timing recovery system in accordance with the present invention.

Figure 5 shows plots of the simulation results of phase locking process for the 100-m cable environment.

Figure 6 shows plots of the simulation results of phase locking process for the 5-m cable environment.

Figure 7 is a block diagram of one embodiment of the timing error detector of Figure 4.

Figure 8 is a block diagram of an alternative embodiment of the timing error detector of Figure 4.

Figure 9 is a block diagram of an another alternative embodiment of the timing error detector of Figure 4.

Figure 10 is a block diagram of an another alternative embodiment of the timing error detector of Figure 4.

The figures depict embodiments of the present invention for purposes of illustration only. One skilled in the art will readily recognize from the following discussion that alternative embodiments of the structures and methods illustrated herein may be employed without departing from the principles of the invention described herein.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

A. Derivation of New Timing Functions

Fig. 1 shows a block diagram of the DFE 101 combined with a feed-forward filter (FFF) 100. The FFF 100, having filter coefficients *w(n)* where n is the sample number, rejects pre-cursors, while the feedback filter (FBF) 102 eliminates post-cursors of the channel impulse response. If the sampled channel impulse response is *h(n)*, then the feedback filter coefficients b(n) satisfy

$$b(n) = \frac{h(n)}{h(0)}, \quad n > 0.$$

After the FBF removes post-cursors, only the channel impulse response is left in the pre-cursors. Then, the received signal at the equalizer input, represented by *x(n)*, is as follows:

$$x(n) = \sum_{i=-\infty}^{0} h(i)a(n-i)$$

where *a(i)* represents transmitted, noiseless data. If the feed-forward filter has N taps and the indexes of the taps decrease from the right-most main tap with index *N-1*, then the filtered output, $\hat{a}(n)$, is obtained as follows:

$$\begin{aligned}\hat{a}(n) &= \sum_{i=0}^{N-1} w(N-i-1)x(n+i) \\ &= \sum_{i=0}^{N-1} w(N-i-1) \sum_{j=-\infty}^{0} h(j)a(n+i-j) \\ &= \sum_{i=0}^{N-1} w(N-i-1) \sum_{j=0}^{\infty} h(-j)a(n+i+j).\end{aligned}$$

After substitution of the sum of the indexes $i+j$ by a new index k, the above equation is reduced to

$$\hat{a}(n) = \sum_{k=0}^{\infty} a(n+k) \sum_{j=0}^{k} w(N-k+j-1)h(-j).$$

The output of the feed-forward filter, $\hat{a}(n)$, is equal to $a(n)$ when perfect equalization is achieved. Under the zero-forcing condition, the terms in the above equation should be zeros except when k is equal to zero.

$$w(N-1)h(0) = 1$$

$$\sum_{j=0}^{k} w(N-k+j-1)h(-j) = 0, \quad k \neq 0.$$

where the main tap and the adjacent tap coefficients of the feed-forward filter are represented by the channel impulse response, $h(n)$, as follows:

$$w(N-1) = \frac{1}{h(0)}$$

$$w(N-2) = -\frac{w(N-1)h(-1)}{h(0)} = -\frac{h(-1)}{h(0)^2}.$$

By combining the coefficients of the main tap130, the adjacent tap 128, and the first feedback filter tap 132, the following timing function can be obtained:

$$z_0(n) = \frac{b(1)}{w(N-1)} + \frac{w(N-2)}{w(N-1)^2} = h(1) - h(-1) \qquad (4)$$

By removing $w(N-1)$ in the denominator of both terms, another timing function is derived as follows:

$$z_1(n) = b(1) + \frac{w(N-2)}{w(N-1)} = \frac{h(1) - h(-1)}{h(0)}. \qquad (5)$$

A division operation usually relies upon more complicated hardware than a

multiplication operation. Therefore, one can derive another timing function that does not use division by multiplying :z_1 by w(N-1) to obtain:

$$z_2(n) = b(1)w(N-1) + w(N-2)$$
$$= \frac{h(1) - h(-1)}{h(0)^2}. \qquad (6)$$

Alternatively, one can derive a timing function that does not involve multiplication of tap coefficients:

$$z_3(n) = k_1 b(1) + k_2 w(N-2)$$
$$= k_1 \frac{h(1)}{h(0)} - k_2 \frac{h(-1)}{h(0)^2}. \qquad (7)$$

where constants k_1 and k_2, should be carefully chosen to balance the inherently different scaling factors of *b(1)* and *w(N-2)*.

For those channels with an asymmetrical impulse response, the above timing functions can be modified by incorporating two scale factors, α and β, as follows:

$$z_0(n) = \alpha_0 \frac{b(1)}{w(N-1)} + \beta_0 \frac{w(N-2)}{w(N-1)^2}$$
$$z_1(n) = \alpha_1 b(1) + \beta_1 \frac{w(N-2)}{w(N-1)}$$
$$z_2(n) = \alpha_2 b(1)w(N-1) + \beta_2 w(N-2)$$
$$z_3(n) = \alpha_3' k_1 b(1) + \beta_3' k_2 w(N-2)$$
$$= \alpha_3 b(1) + \beta_3 w(N-2).$$

Fig. 7 is a block diagram of one embodiment of the timing error detector 120 of Fig. 4 according to the timing function $z_0(n)$. The first post-cursor b(1) and the main tap, w(N-1), are the a and b inputs, respectively, of an a/b divider 134. The output of the a/b divider 134 is the input of an amplifier 136 for scaling the output of the a/b divider 134 by a factor of α_0. The output of the amplifier 136 is the first of two inputs to a summing logic 144.

The main tap, w(N-1) is also the input to a squaring device 138. The first pre-cursor, w(N-2), and the output of the squaring device are the a and b inputs, respectively, to a a/b divider

140. The output of the a/b divider 140 is the input to an amplifier 142 for scaling the output of the a/b divider 140 by a factor of β_0. The output of the amplifier 142 is the second of two inputs to the summing logic 144. The output of the summing logic 144 is the timing function $z_0(n)$ and is the output of this embodiment of the timing error detector.

Fig. 8 is a block diagram of another embodiment of the timing error detector 120 of Fig. 4 according to the timing function $z_1(n)$. The first post-cursor, b(1), is the input to amplifier 136 for scaling the post-cursor by a factor of α_1. The output of the amplifier 136 is the first of two inputs to a summing logic 144.

The first pre-cursor, w(N-2), and the main tap, w(N-1), are the a and b inputs, respectively, for an a/b divider 140. The output of the a/b divider 140 is the input of an amplifier 142 that scales the output of the a/b divider 140 by a factor of β_1. The output of the amplifier 142 is the second of two inputs to the summing logic 144. The output of the summing logic 144 is the timing function $z_1(n)$ and is the output of this embodiment of the timing error detector.

Fig. 9 is a block diagram of another embodiment of the timing error detector 120 of Fig. 4 according to the timing function $z_2(n)$. The first post-cursor, b(1), and the main tap, w(N-1), are the a and b inputs, respectively to an a/b divider 134. The output of the a/b divider 134 is the input to amplifier 136 for scaling the post-cursor by a factor of α_2. The output of the amplifier 136 is the first of two inputs to a summing logic 144.

The first pre-cursor, w(N-2), is the input of an amplifier 142 that scales the first pre-cursor by a factor of β_2. The output of the amplifier 142 is the second of two inputs to the summing logic 144. The output of the summing logic 144 is the timing function $z_2(n)$ and is the output of this embodiment of the timing error detector.

Fig. 10 is a block diagram of another embodiment of the timing error detector 120 of Fig. 4 according to the timing function $z_3(n)$. The first post-cursor, b(1), is the input to amplifier 136 for scaling the post-cursor by a factor of α_3. The output of the amplifier 136 is the first of two inputs to a summing logic 144.

The first pre-cursor, w(N-2), is the input of an amplifier 142 that scales the first pre-cursor by a factor of β_3. The output of the amplifier 142 is the second of two inputs to the summing logic 144. The output of the summing logic 144 is the timing function $z_3(n)$ and is the output of this embodiment of the timing error detector.

A s will be clear to those of skill in the art, a variety of other embodiments of the timing error detector are possible in hardware and/or software. The embodiments described above are intended to be illustrative and not limiting

B. Characteristics of New Timing Functions

The scale factors shown above should be chosen properly according to the channel environment when the impulse response of the channel is asymmetrical. Fig. 2 shows the impulse response of the 100m-length UTP Category-5 cable including the effect of a digital shaping filter having a filtering function = $0.75+0.25z^{-1}$ (where z is the complex impedance), of an analog low-pass transmit/receive filter, and of a hybrid transformer with a cut-off frequency of 200kHz. For more details, see *Physical layer specification for 1000 Mb/s operation on four pairs of Category 5 or better balanced twisted pair cable*, IEEE Std 802.3ab, 1998, which is incorporated by reference in its entirety herein. The asymmetric characteristics of the UTP Category-5 cable appear regardless of its length. Table I shows the value of first post-cursor and pre-cursor of the UTP Category-5 cable with a varied length.

TABLE I: **THE FIRST POST-CURSOR AND PRE-CURSOR OF THE IMPULSE RESPONSE OF THE UTP CATEGORY-5 CABLE WITH EXTERNAL EFFECTS.**

Cable length	h(-1)	h(0)	h(1)
5m	0.00013	0.67	0.23
10m	0.00015	0.66	0.24
20m	0.00011	0.60	0.24
30m	0.0016	0.54	0.24
40m	0.0027	0.48	0.24
50m	0.0063	0.43	0.23
60m	0.011	0.38	0.22
70m	0.016	0.34	0.21
80m	0.021	0.3	0.20
90m	0.027	0.27	0.19
100m	0.040	0.21	0.14

The suitable scale factors of the timing functions for the channels in Table I are listed in Table II.

TABLE II: **THE SCALE FACTORS OF TIMING FUNCTIONS.**

Cable length	α_0, α_1, α_2, α_3	β_0, β_1, β_2	β_3
5m	1	1769	1185
10m	1	1600	1072
20m	1	2182	1309
30m	1	150	81
40m	1	89	43
50m	1	37	16
60m	1	20	7.6
70m	1	13	4.5
80m	1	9.5	2.9
90m	1	7.0	1.9
100m	1	3.5	2.2

α and β are selected to yield a zero for each timing function when in the optimal timing phase. In other words, to obtain the ratio between α and β, one inserts the measured values for h(1), h(0), and h(-1) from table I into equations 4, 5, 6, and 7 above, the equations having been modified so that the first term is multiplied by α and the second term is multiplied by β. Then one sets the resulting equations equal to zero and solves for the ratio of α and β. Having obtained the ratio, one can set $\alpha = 1$ to obtain β. In this way, one selects α and β to provide a zero correction when in the timing phase is optimal. Detector characteristics of the timing functions with scale factors for the impulse response of the 100-m UTP Category-5 cable are plotted in Fig. 3. Although they are not monotonic for a small range of sampling phases, all four timing functions show linear characteristics around the zero phase or at the optimum sampling phase.

C. Timing Recovery System with Phase Locked Loop

A timing recovery system consists of a timing error detector 120, a loop filter 122, and a voltage-controlled oscillator (VCO) 124 to form a Phase-Locked Loop (PLL). Fig. 4 shows a block diagram of one embodiment of the invention, where the timing error detector 120 uses one of the timing functions derived above. Although digitally controlled VCOs or Numerically Controlled Oscillators (NCOs) are available, an analog loop filter and a VCO may also be incorporated.

The transfer function of the loop filter, $H_{loop}(s)$, and the transfer function of the VCO, $H_{VCO}(s)$, are

$$H_{loop}(s) = K_1 + \frac{K_2}{s}$$

$$H_{VCO}(s) = \frac{K_{VCO}}{s}.$$

where K1 and K2 are arbitrary constants and Kvco is a constant for the VCO and s represents frequency. For more details, see *Synopsys Online Documentation-Designing Synchronization Subsystems in COSSAP*, Synopsys, Inc., 1998, which is incorporated by reference herein in its entirety.

The overall closed loop transfer function, $H(s)$, is

$$H(s) = \frac{1}{1 + K_t K_{VCO} H_{loop}(s)/s}$$

where K_t is the gain of the timing error detector. The damping ratio, ξ, and the normalized loop bandwidth, BL, have the following relationship

$$\omega_n^2 = K_t K_{VCO} K_2$$

$$\xi = \frac{K_t K_{VCO} K_1}{2\omega_n}$$

$$BL = \frac{\omega_n}{2}(\xi + \frac{1}{4\xi})$$

where ω_n is a natural frequency of the system. K_1 and K_2 should be chosen to satisfy the desired damping ratio and the loop bandwidth. These equations allow for the calculation of K1 and K2. For more details, see H. Meyr and G. Ascheid, *Synchronization in Digital Communication Volume 1*, Wiley Series, which is incorporated by reference in its entirety herein.

The timing functions are derived from the feed-forward and feedback filter coefficients with varying amounts of computation. The functions are based on the derived relations between the coefficients of feed-forward and feedback filters and the channel impulse response. The most complex timing function would need two divisions, three multiplications, and one addition, whereas the least complex one would need only two multiplications and one addition.

D. Simulation Results

FIGS 2, 5, and 6 and Tables I and II show the results of the simulated performance of the four timing functions described above. The simulated performance used 125-M Baud signaling with 100-m and 5-m UTP Category-5 cables. FIG. 2 shows the channel impulse. The gains of the derived timing functions, K_t, are 0.32, 0.60, 1.16, and 0.74, respectively. K_{VCO} has the normalized value of 1, and K_1 and K_2 were selected as 0.001 and 0.0000001, respectively. In the simulations, the free running frequency of the VCO is displaced from the transmitter clock frequency by 200 parts per million (ppm).

Fig. 5 shows the frequency locking process of the VCO and the acquisition of the sampling phase when $z_0(n)$, $z_1(n)$, $z_2(n)$, and $z_3(n)$ are used as timing functions with varied initial sampling phases from -0.5 to 0.5. Since the impulse response is not symmetrical, the scale factor of $z_0(n)$ for a 100-m cable shown in Table II is used.

For equalization, the following decision-directed algorithm is incorporated to work jointly with the timing recovery

$$y(n) = \sum_{i=0}^{N-1} w_n(i)x(n+N-1+i) + \sum_{i=1}^{M} b_n(i)\hat{y}(n-i)$$
$$e(n) = \hat{y}(n) - y(n)$$
$$w_{n+1}(i) = w_n(i) + \mu e(n)x(n+N-1+i) \quad i = 0, \cdots, N-1$$
$$b_{n+1}(i) = b_n(i) + \mu e(n)\hat{y}(n-i) \quad i = 1, \cdots, M$$

where *y(n)* is filtered output, *ŷ(n)* is the nearest decision value, and *N* and *M* correspond to the number of taps in feed-forward and feedback filters, respectively. To assure the convergence of the decision-directed algorithm, the coefficient of the main tap, *h(0)*, is initialized to a high value considering the variations of the channel impulse response See G. J. Foschini, "Equalization without altering or detecting data," *AT&T Technical Journal*, vol. 64, pp. 1885-1911, Oct. 1985, which is incorporated herein by reference in its entirety. Blind equalization algorithms may also be used without altering the timing functions. A blind equalization algorithm is an equalization algorithm that does not enjoy the benefit of a training sequence.

Figs. 5 (a), 5(c), 5(e), and 5(g) show the output of the loop filter. Since the free running frequency of the VCO clock of the receiver is slower than the transmitter clock by 200 ppm, the output of the loop filter should be 0.0002 when the frequency lock is reached. In Figs. 5 (b), 5(d), 5(f), and 5(h), the sampling phase is normalized to 2π so that $-\pi$ and π correspond to -0.5 and 0.5, respectively. Thus, the sampling phase should be settled at an integer value when the phase lock is reached.

In most cases, since the channel impulse response is not known beforehand, the scale factors cannot be determined. However, based on the present simulations, one can estimate the worst-case impulse response, and one can use scale factors based on the worst case estimate without any severe degradation in performance. Simulation results for the 5-m cable (best case) with the scale factors obtained from the 100-m cable (worst case) are shown in Fig. 6.

Frequency lock with the timing offset of less than 0.1 is reached with a negligible degradation in SNR.

The simulations show that frequency lock and phase lock are reached in less than 20,000 symbols with a settling behavior typically found in adaptive systems. The simulation results show that all of the timing functions derived work robustly in a severely distorted channel as well as in a moderately distorted one when they are incorporated in a PLL with decision-directed equalization. The PLL's lock is reached in less than 20,000 symbols for all the timing functions and under all initial conditions with the steady-state phase offset of less than 0.1 symbol time.

Another advantage of embodiments of the present invention is the reduction in noise enhancement. As noted above, a linear equalizer includes a number of taps, each tap time delayed relative to its neighbor, the taps measuring the input. The linear equalizer multiplies the output of the taps by coefficients and sums the resulting terms. Thus, the equalizer also multiplies the Gaussian noise term in the input by the same coefficients and sums the resulting terms to increase the noise power. Consequently, Noise power is proportional to the number of taps. On the other hand, a DFE consists of a FFF and a FBF and the input to the FBF is noiseless because the input to the FBF is from a slicer. Thus, the number of taps in a FFF is fewer than that in a linear filter. As a result, a DFE has less noise enhancement than a linear filter.

While the invention has been described with reference to preferred embodiments, it is not intended to be limited to those embodiments. It will be appreciated by those of ordinary skilled in the art that many modifications can be made to the structure and form of the described embodiments without departing from the spirit and scope of this invention.